This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

a wiring layout where ~~wirings not to be electrically shorted are crossed~~crossed wirings ~~is~~ are implemented by a two-layer wiring structure, to avoid electrical shorts.

2. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), anodes or cathodes of n light-emitting thyristors included in each block are separately connected to n anode-selecting lines or cathode-selecting lines, and gates of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

a wiring layout where ~~wirings not to be electrically shorted are crossed~~crossed wirings ~~is~~ are implemented by a two-layer wiring structure, to avoid electrical shorts.

3. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

a wiring layout where ~~wirings not to be electrically shorted are crossed~~crossed wirings ~~is~~ are implemented by utilizing gate electrodes of the light-emitting thyristors as cross under wirings, to avoid electrical shorts.

4. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), anodes or cathodes of n light-emitting thyristors included in each block are separately connected to n anode-selecting lines or n cathode-selecting lines, and gates of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

a wiring layout where ~~wirings not to be electrically shorted are crossed~~crossed wirings ~~is~~ are implemented by utilizing anode electrodes or cathode electrodes of the light-emitting thyristors as cross under wirings, to avoid electrical shorts.

5. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

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bonding pads ~~are~~ arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

a wiring layout where ~~wirings to~~a crossed wiring between the bonding pads ~~cross~~ and the gate-selecting lines is implemented by utilizing, as a cross under wiring, ~~electrodes~~ at least one of an anode electrode and a cathode electrode on an ~~on~~ islands that is isolated from the light-emitting thyristors ~~as cross under wirings~~, to avoid electrical shorts.

6. (Currently Amended) The light-emitting thyristor matrix array of claim 5, wherein the electrodes on the islands isolated from the light-emitting thyristors ~~are~~ include at least one of a gate electrodes, an anode electrodes, ~~or~~ and a cathode electrodes.

7. (Currently Amended) The light-emitting thyristor matrix array of claim 5, wherein at least one of the anode electrode ~~or~~ and cathode electrode is utilized as the cross under

wiring, and at least one of the anode electrode ~~or~~ and cathode electrode is electrically shorted to the gate electrode on the same isolated island.

8. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

bonding pads ~~are~~ arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

A1 Cont.

a wiring layout where ~~wirings to~~a crossed wiring between the bonding pads ~~cross~~ and the gate-selecting lines is implemented by utilizing, as a cross under wiring, a gate electrode elongated around a light-emitting portion of the thyristor ~~as a cross under wiring~~, to avoid electrical shorts.

9. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), gates of n light-emitting thyristors included in each block are separately connected to n gate-selecting lines, and anodes or cathodes of n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

bonding pads ~~are~~ arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

a wiring layout where ~~wirings to~~a crossed wiring between one of the bonding pads ~~cross~~ and one of the gate-selecting lines is implemented by utilizing two gate electrode parts provided around a light-emitting portion of the thyristor as a cross under wiring, the two gate electrode parts being electrically connected by an underlying gate layer, to avoid an electrical short.

10. (Currently Amended) A light-emitting thyristor matrix array wherein an array of three-terminal light-emitting thyristors in which a substrate that is used as a common cathode or anode is divided into blocks of n by n (n is an integer ≧ 2), anodes and cathodes of n light-emitting thyristors included in each block are separately connected to n anode-selecting lines or cathode-selecting lines, and gates of the n light-emitting thyristors included in each block are commonly connected to one terminal, respectively, characterized ~~in that~~by:

bonding pads ~~are~~ arrayed in parallel with the array direction of the light-emitting thyristors and on one side of the array of the light-emitting thyristors, and

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a wiring layout where ~~wirings to~~ crossed wirings between the bonding pads ~~cross~~ and ones of the anode-selecting lines ~~or~~ and cathode-selecting lines ~~is~~ are implemented by utilizing, as cross under wirings, electrodes on islands that are isolated from the light-emitting thyristors ~~as cross under wirings~~, to avoid electrical shorts.

11. (Original) The light-emitting thyristor matrix array of claim 10, wherein the electrodes on the islands isolated from the light-emitting thyristors are gate electrodes, anode electrodes, and cathode electrodes.

12. (Currently Amended) The light-emitting thyristor matrix array of claim 11, wherein at least one of the anode electrodes ~~or~~ and the cathode electrodes is utilized as the cross under wiring, and the at least one of the anode electrodes ~~or~~ and the cathode electrodes is electrically shorted to the gate electrode on the same isolated island.